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Field Programmable Gate Array (FPGA) based implementation of efficient RC6 block cipher

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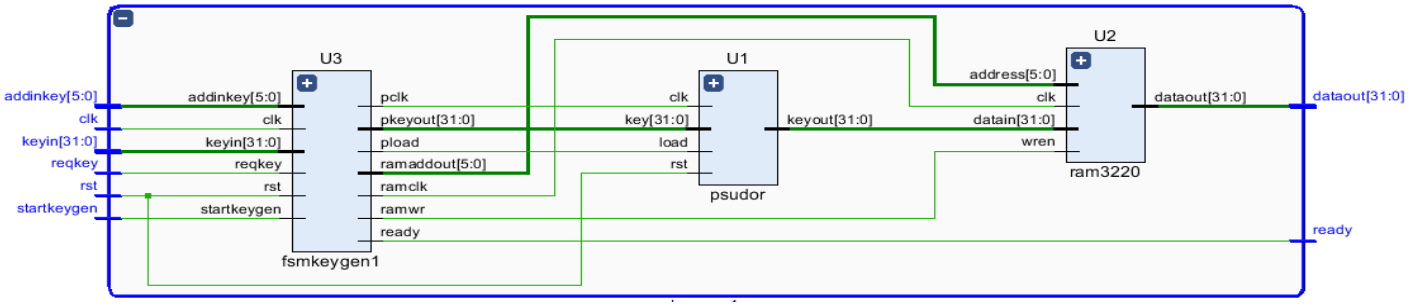
ABSTRACT



The efficient encryption system is required to achieve goal of security services. Rivest cipher 6 is a symmetric key block cipher which incorporates data dependent rotations. RC6 is specified as RC6-w/r/b, where the parameters w, r, and b respectively express the word size (in bits), the number of rounds, and the size of the encryption key (in bytes). In current work, optimized RC6 is implemented using xc7vx330t-2-ffg1157 field programmable gate array with proposing of inclusion of RC6-32/20/16. High value of rounds creates more diffusion and enables more security. Proposed system is synthesized and implemented on virtex7 field programmable gate array. The proposed method has less resource utilization and high throughput. Resource utilization in terms of slices is only 1% and in terms of fully used LUT-FF pair is 15%. Throughput of proposed system is 99.22 Gbps and efficiency is 50.596 Mbps/slice. Security analysis by performing avalanche test and strict avalanche criterion is also done. Average Avalanche effect of 54.71 is achieved, which satisfies criteria of SAC.

Keywords: RC6, Avalanche effect, Field programmable gate array, throughput, barrel shifter

INTRODUCTION

The deployment of computer-based information system is continuously increasing in various sectors like e-commerce, health care, eduaction, smart agricultural and social networks. Advances in internet of things (IoT) and big data eanbles data sharing for different applications.[1–4] Next generatin cellular systems also leades to high data rate due to which data exchange also increases. For all such cases data privacy and security is a major concern.[5] At various levels from indivdual, group, organization and society there is big concern of security and privacy of information.[6] Efficient secure and privacy scheme is the solution to this issue.[7] Such efficient RC6 algorithm is proposed in this work. RC6 is symmetric key[8] modern block cipher derived from RC5. Field Programmable Gate Arrays (FPGA) implementaion of encryption algorithm for various applications is preferred.[3,9–11] Encryption process mainly envolves pre-whitening, an inner loop of rounds, and post-whitening.[12] Reconfigurable architecture and processor-based design gives a strong system level design[13] which is used to handle networking. Virtex7[14] Field programmable gate array is used to implement proposed work and optimization is carried out to get high throughput and high efficiency. Synthesis and implementation of RC6-32/20/16 using xc7vx330t-2-ffg1157 is done. Very-large-scale integration (VLSI) design constants in terms of area, speed and memory usage were achieved efficiently.

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The review of related work conducted to is given in second section.Description of proposed methodology with details of each process is elaborated in next section.Later results obtained after synthesis and implementation process are discussed.Results of avalanche effect test and SAC are also discusssed. Last section gives comprative analysis and conclusion of research work.

Related work

RC6 modules

RC6 encrypts plaintext in fixed-size 128-bit blocks. RC6 is a fully parameterized family of encryption algorithms. A version of RC6 is more accurately specified as RC6-w/r/b where the word size is w bits, encryption consists of a non-negative number of rounds as r, and b denotes the length of the encryption key in bytes. RC6 works with 4 w-bit registers A, B, C, D which contain the initial input plaintext as well as the output cipher text at the end of encryption process. For high security higher value of round is selected. RC6 working is divided into three main modules as key generation module, encryption module and decryption module. The key expansion algorithm is used to expand the user-supplied key to fill an expanded array S, so S resembles an array of *r* random binary words. Encryption process as shown in figure 1. Register B and D undergoes process of pre whitening.The resulting value of B after rotation has an exclusive-or operation with A, and D with C respectively. In the final stage of the round, the register values are permuted. At last stage registers A and C undergo post-whitening process using S array.

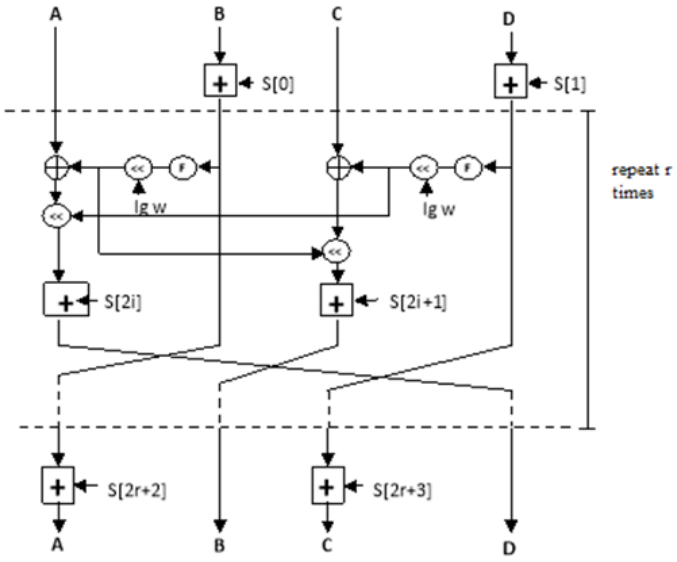


Figure 1. RC6 encryption process

Many reseacher had work on RC6 using various hardware and software platforms. Author designed RC6-Cascade which is 320-bits RC6 like block cipher and its implementaion on Altera FPGA gives improved avalanche efffect. Plaintext is divided into five parts and cascaded design is used.[15] Author had proposed light version of RC6 , RC6 8/5/b as RC6-lite and implemented using Microsoft Visual Basic Express Edition.[16] Compact hardware design of RC6 is propsed by author[17] using VirtexII FPGA. Resuse of same units for identical operation is done. Investigation and implementations of the f(X) operator of RC6 on Virtex-E and Virtex-II devices is done by authors. Design for feedback or non-feedback chaining modes is also done. Due to appropriateness for real-time applications RC6 is used for color image cryptosystem.[18] Cipher block chaining, cipher feedback, and output feedback modes can efficiently and effectively be used for color image encryption. RC6 technique is implemented in Cipher Feedback mode of operation as a first step for encrypting the multiple 3D video frames.[19] The mode of cipher-block chaining used by author. The practical performance was measured on a 2.40GHz Intel(R) Core(TM) i3 CPU with 4GB of RAM running Windows XP. Confusion, CPU utilization and memory utilization for Rijndael and RC6 algorithms is compared by author. RC6 is mostly suitable for these occasions where high encryption speed is required while Rijndael is useful where memory resource is key concern.[20,21] Author had proposed dynamic keys generation from the RC6 algorithm mixed with RC4 to create dynamic S-box and permutation table which preventes several known attacks during the real-time data transmission.[22]

Proposed methodology

Implementation of RC6 using pipeline structure is proposed in this work. As pipeline method includes a register in between two rounds, data is fetched continously which increases speed of operations. Design, implementation, simulation and synthesis is done on xc7vx330t-2-ffg1157 Field programmable Gate array using Xilinx 14.7 ISE and Aldec active HDL. Comparative analysis with existing work in terms resource usage, throughput and efficiency is done. Proposed modules are elaborated in following section.

Key expansion module

Key expansion module is used to expand the used defined key to fill an expanded array S, so S resembles an array of random binary words. Initially selection of two constants P and Q is done as

$$P = Odd((e-2)2^w) \quad (1)$$

$$Q = Odd((\phi-1)2^w) \quad (2)$$

Where e is base of natural logarithms and ø is golden ratio whose values are 2.718 and 1.6180 respectively. Odd(x) is the least odd integer greater than or equal to |x|. Process of key expansion is as per pseudocode 1.Output of this module is w-bit round keys S[0,…, 2r + 3]. In proposed work round r is 20, hence output is round keys S[0,1,--,43].

Pseudocode 1:

```
S[0]=P
for i=1 to 43 do
S[i]=S[i-1]+Q
X=Y=i=j=0
v=3*max{4,44}=132
for s=1 to 132 do
{
X=S[i]=(S[i]+X+Y)<<<3
Y=L[j]=(l[j]+X+Y)<<<(X+Y)
i=(i+1) mod 44
j=(j+1) mod 4
}
End
```

This module is implemented using vivado 17.4,Aldec active-HDL and synthesis is done using xilinx 14.7.Fig 2 shows RTL schematic of key generation module.

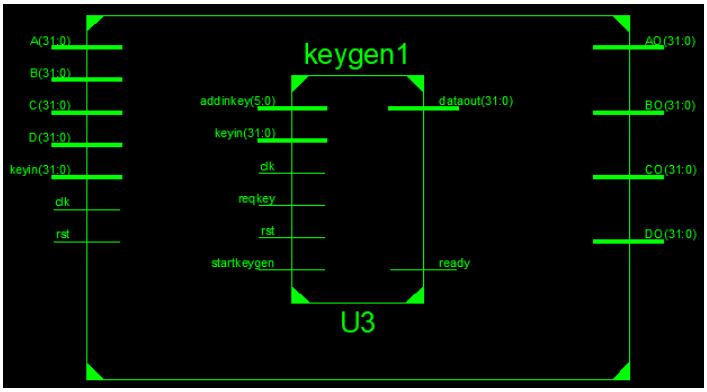


Figure 2. RTL schematic of key generation process

Encryption module

The processes of encryption and decryption are both composed of three stages: pre-whitening, an inner loop of rounds, and post-whitening. Main focus of proposed method is reuse of modules for compact design. So efficient design of the intermediate stages is done. Encryption process is as given pseudocode 2. Input given is plaintext stored in four w-bit input registers A,B,C,D number r of rounds and w-bit round keys S[0,…,2r + 3] where r is 20.

Pseudocode 2.

```
 B=B+S[0]
D=D+S[1]
for i=1 to 20
{
t=(B*(2B+1))<<<5
u=(D*(2D+1))<<<5
A=((A xor t)<<<u)+S[2i]
C=((C xor u)<<<t)+S[2i+1]
(A,B,C,D) = (B,C,D,A)
}
A=A+S[42]
C=C+S[43]
End
```

The registers B and D uses quadratic equation and rotated ($\log_2$ w) bits to the left, respectively. The resulting value of B has an exclusive-or operation with A, and D with C respectively. This value *t* is then left-rotated *u* bits and added to round key. The resulting value of D and C is left-rotated *t* bits and added to round key S[2i + 1]. In the final stage of the round, the register values are permuted, using parallel assignment process.

Decryption Module

Decryption module exhibits structure similarity with encryption module whereas reverse procedure is performed. Intially pre whitening process on C and A registers is carried out. Loop execution is in reverse for the r rounds. In loop execution firstly parallel assignment is done. Qurdratic equation is applied on D and B and resulting values are stored in u and t subregisters. These values are then left rotated. Steps performed are as per Pseudocode 3. After performance of all iterations finally D and B undergoes post-whitening process.

Pseudocode 3:

```
C=C-S[43]
B=B-S[42]
for i=20 downto 1
{
(A,B,C,D) = (D,A,B,C)
u=(D*(2D+1))<<<5
t=(B*(2B+1))<<<5
C=((C-S[2i+1])>>>t) xor u
A=((A-S[2i])>>>u) xor t
}
D=D-S[1]
B=B-S[0]
End
```

Implementation of operators used in RC6

Main operators used in RC6 implementation are given in table 1. Efficient design of these repetative operators is done in the proposed work. Implementation of carry look ahead adder and subtractor is done. The carry term is expanded recursively to each step to provide a 32-bit carry look-ahead adder substractor. The carry expression for each individual stage can be implemented in a two-level AND-OR expression. For rotation operation 32 bit right-left rotate by concatenating 1'b0 with 32-bit input word. Implementation of shift and add multiplication algorithm consists of looking at each successive bit of the multiplier in turn, starting with the lsb. A barrel shifter is a circuit which can shift a data word by a specified number of bits in one clock cycle. Implementation of barrel shifter is done as a cascade of parallel 2×1 multiplexers. RTL schematic of barrel shifter is as shown in figure 3. For a 4-bit barrel shifter, an intermediate signal is used which shifts by two bits, or passes the same data based on value of s[0] or s[1].

Table 1 Operators used in RC6

Operation	Description
a $\oplus$ b	Bitwise exclusive-or of w-bit words
a x b	Integer multiplication modulo 2^w
a <<< b	Rotate the *w*-bit word a to the left by the amount given by the least significant ($\log_2 w$) bits of *b*
a >>> b	Rotate the *w*-bit word a to the right by the amount given by the least significant ($\log_2 w$) bits of *b*
Enc: (A,B,C,D) = (B,C,D,A) **Dec:** (A,B,C,D) = (D,A,B,C)	Parallel assignment of values on the right to registers on the left.

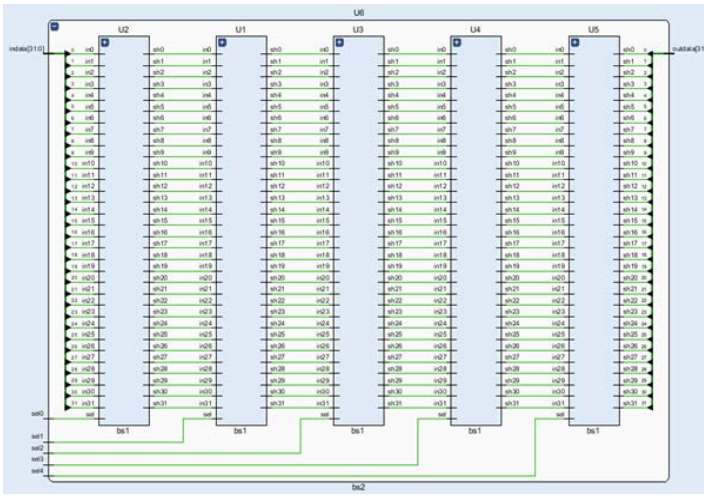


Figure 3: Barrel shifter RTL schematic

RESULTS AND DISCUSSION

The simulation and synthesis was performed to check correctness of the proposed design. Synthesis, simulation and Implementation results for proposed optimized method were analyzed. Resource utilization is as shown table 2. Simulation of modules done individually and then complete pipeline RC6 system is simulated using Aldec active HDL. Simulation waveform is shown in figure 4.

Figure 4. Output simulation waveforms

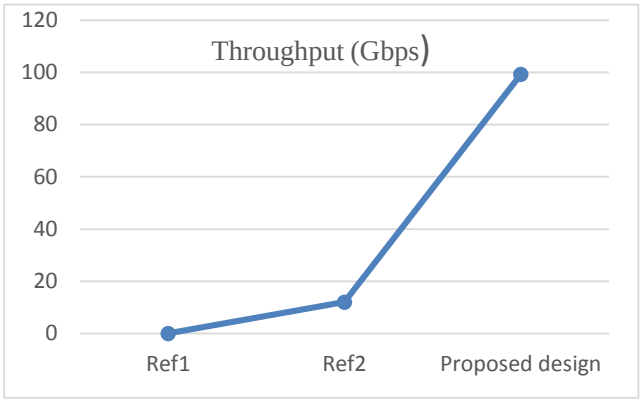
Table 2. Resource utilization

Parameters	Used in the proposed design	Available	% Utilization
No.of slice registers	1961	408000	1%
No.of slice LUTs	2145	204000	1%
No.of fully used LUT-FF pair	558	3548	15%
No of bonded IOB	289	600	45%

As given in table 2, only 1% slices are used which satisfies area constraints very effectively. Number of slice LUTs utilization is only 1%. Look up table- flip flop pair utilization is 15%. Bonded input output buffer utilization is 45%. Other parameters which plays very important role in analysis of algorithm are listed in table 3. Throughput is the ratio of number of processed bits and critical delay. Throughput also decides efficiency of system. It is calculated as ratio of throughput and number of slices used. Proposed design gives throughput 99.22 Gbps which is very high as compared to existing reference work ref 1 and ref 2,[23,24] where throughput is 0.0039 Gbps and 12 Gbps respectively. Efficiency of the design is 50.596 Mbps/Slice.

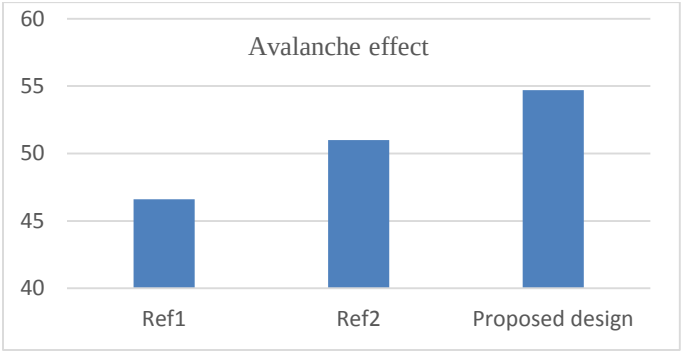
Table 3. Result summary

Parameters	Proposed design
Memory	480 MB
Critical Delay	1.29 ns
Frequency	770.89 MHz
Throughput	99.22 Gbps
Efficiency	50.596 Mbps/Slice
Plaintext Avalanche effect (Average)	54.12
Key Avalanche effect (Average)	55.3



Graph 1.Comparative analysis of throughput

Security of encryption method is analyzed by avalanche effect test. Avalache effect measues changes in ciphertext that occur when plaintext or key changes by one bit.[25] High avalanche effect guarantees security of plaintext. Tests have been carried out by change in key and change in plaintext. Average avalanche effect of 54.12 and 55.3 is obtained for one bit change in key and one bit change in plaintext respectively. More avalanche effect is obtained in this work as compared to existing work[26,15] where avalanche effect of 46.6 and 51 is obtained.



Graph 2. Avalanche effect analysis

As avalanche effect is more than 50% it satisfies strict avalanche criterion. It proves that proposed method has good diffusion

characteristics. Proposed system also passess frequency test and runs test which are used for validation. Statistical analysis gives P-Value 0.7. High p-Value indicated randomness in the output.

CONCLUSIONS

High throughput and efficiency are key features of encryption algorithms. In proposed work optimized RC6 implementation on FPGA device is done. Pipeline method and efficient modules design achieves constraints of area and speed. Only 1% slice registers and 1% slice LUTs are used in the design. LUT-FF pair usage is 15%. Critical delay observed is 1.29 ns. Maximum frequency achieved is 770.89MHz. High throughput of 99.22 Gbps is achieved. Average avalanche of 54.71 proves that method is secure and strict avalanche criterion is satisfied. High efficiency makes proposed work suitable for real time applications. Tests specified by National Institute of Standard and Technology(NIST) are performed and executed effectively to validate proposed work.

CONFLICT OF INTEREST

Authors declared no conflict of interest.

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